A SOLUTION TO THE PROBLEM OF COPPER HILLOCKS

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention relates to a method of copper metallization in the fabrication of integrated circuits, and more particularly, to a method of reducing the formation of copper hillocks in copper metallization in the manufacture of integrated circuits.

(2) Description of the Prior Art

In a common application for integrated circuit fabrication, a contact/via opening is etched through an insulating layer to an underlying conductive area to which electrical contact is to be made. A conducting layer material is deposited within the contact/via opening. Because of its lower bulk resistivity, Copper (Cu) metallization is the future technology for feature sizes of 0.18 microns and below. Often, a damascene or dual damascene process is used to provide Cu metallization. The copper is deposited within the damascene opening and polished back. Then, a capping layer, such as silicon nitride or silicon carbide, is deposited over the copper plugs to prevent copper from diffusing into overlying layers.

Typically, before the capping layer is deposited, the wafer is heated to stabilize the wafer temperature. A coating of the capping layer material on the deposition chamber walls releases NH_x-related molecules that react with copper to cause Cu hillock generation. Cu hillocks are also caused by exposing the wafers to NH_3 gas in the ambient of the deposition chamber. Copper hillocks reduce copper reliability and confuse defect inspection tools. Reduction of copper hillocks in the copper damascene process becomes more and more important for yield and reliability improvement. It is desired to reduce copper hillock generation in the copper metallization process.

U.S. Patent 5,714,418 to Bai et al discloses a capping layer of nitride over copper, then an oxide layer. U.S. Patent 5,612,254 to Mu et al a silicon nitride layer over copper. U.S. Patent 5,654,232 to Gardner teaches a copper damascene process. U.S. Patent 5,589,233 to Law et al shows a chamber pre-coat process. None of the references discusses Cu hillock prevention.

SUMMARY OF THE INVENTION

A principal object of the present invention is to provide an effective and very manufacturable method of

reducing copper hillocks in a copper metallization process in the fabrication of integrated circuit devices.

Another object of the invention is to provide a method for reducing copper hillocks by reducing copper oxide formation.

A further object of the invention is to provide a method for reducing copper hillocks by pre-coating the deposition chamber with an oxide layer.

A still further object of the invention is to provide a method for reducing copper hillocks by using NH_3 plasma rather than NH_3 gas for CuO reduction after copper chemical mechanical polishing (CMP).

Yet another object of the invention is to provide a method for reducing copper hillocks by reducing the time between copper CMP and capping layer deposition to less than one day.

Yet another object of the invention is to provide a method for reducing copper hillocks by reducing the time between copper CMP and capping layer deposition to less than one day, pre-coating the deposition chamber with an

oxide layer, and using NH_3 plasma rather than NH_3 gas for CuO removal.

In accordance with the objects of this invention a new method of reducing copper hillocks in copper metallization is achieved. An opening is made through a dielectric layer overlying a substrate on a wafer. A copper layer is formed overlying the dielectric layer and completely filling the opening. The copper layer is polished back to leave the copper layer only within the opening. Copper hillocks are reduced by: coating the deposition chamber with an oxide layer, thereafter heating the wafer using NH_3 plasma, and thereafter depositing a capping layer overlying the copper layer and the dielectric layer wherein the time lapse between polishing back the copper layer and depositing the capping layer is less than one day (24 hours).

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings forming a material part of this description, there is shown:

Figs. 1 through 5 schematically illustrate in cross-sectional representation a preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention provides a method for reducing copper hillocks. Hillocks reduce copper reliability and confuse defect inspection tools. Recent studies have shown that copper hillock generation after silicon nitride deposition is caused by the sensitivity of the copper surface to the deposition environment and a low copper oxide (CuO) reduction rate. After the wafer is heated to 400 °C in the deposition chamber, copper grain growth is effected by the chamber pre-coat material and by the presence of CuO.

Referring now more particularly to Fig. 1, there is illustrated a portion of a partially completed integrated circuit device. There is shown a semiconductor substrate 10, preferably composed of monocrystalline silicon. Semiconductor devices structures may be formed in and on the semiconductor substrate. For example, gate electrodes and source/drain regions as well as lower levels of metallization may be formed. The semiconductor device structures, not shown, are contained in layer 14.

An insulating layer 20, composed of silicon dioxide, borophosphosilicate glass (BPSG), borosilicate glass (BSG), phosphosilicate glass (PSG), or the like, is deposited

over the semiconductor structures to a thickness of between about 100 and 10,000 Angstroms and preferably planarized.

A contact/via opening 22 is etched through the insulating layer 20 to one of the semiconductor device structures within the layer 14, not shown. The opening 22 may be a single or dual damascene opening, for example.

Now, a barrier layer may be deposited, not shown. A copper layer 30 is deposited to fill the opening 22, as shown in Fig. 2. The copper layer may be deposited by physical or chemical vapor deposition, electroplating, or electroless plating, for example.

Referring now to Fig. 3, the copper layer is polished such as by chemical mechanical polishing (CMP) to leave the copper layer only within the opening.

Now, a capping layer is to be deposited over the copper line to prevent copper diffusion. Typically, a silicon nitride or silicon carbide layer, for example, is deposited over the copper line. First, the wafer is heated in a plasma-enhanced chemical vapor deposition (PECVD) chamber to stabilize the wafer temperature. Both the pre-coat and the presence of CuO in the chamber have been found

to increase the generation of copper hillocks, as discussed above.

A key to reducing hillocks is to reduce CuO prior to heating the wafer. Typically, NH_3 gas is present in the deposition chamber to generate the H gas that will reduce CuO to Cu. NH_3 plasma has a higher CuO reduction rate than does NH_3 gas. This is because NH_3 plasma has a higher H atom generation rate. Therefore, the process of the present invention uses NH_3 plasma in the deposition chamber to heat the wafer to between about 200 and 600 °C and to more efficiently reduce CuO to Cu. For example, N_2 is flowed at about 1000 sccm while NH_3 is flowed at about 4000 sccm. 13.5 6 MHz radio frequency power is at about 500 watts and a pressure of about 2 Torr is maintained to generate the NH_3 plasma of the present invention.

Also within the chamber prior to heating the wafer, an oxide layer 32 is pre-coated on the chamber walls and on the wafer as illustrated in Fig. 4. The oxide layer is coated to a thickness of between about 10 and 10,000 Angstroms. The oxide pre-coat of the chamber walls reduces copper hillock generation because the oxide will not react with the NH_3 residues in the chamber to form copper hillocks. Without the oxide coating the chamber walls, the capping

layer would coat the chamber walls. The capping layer will react with the NH_3 residues to form copper hillocks.

Now, as shown in Fig. 5, a capping layer 34 is deposited over the pre-coating 32. The capping layer comprises silicon nitride or silicon carbide, for example, having a thickness of between about 100 and 2000 Angstroms. This completes the copper metallization. Hillocks are reduced in the process of the invention. Processing now continues as is conventional in the art. For example, higher levels of metallization may be fabricated. The post-copper CMP processing of the present invention may be used in subsequent copper levels to further reduce copper hillocks.

Additionally, it is important that the time between copper CMP and the capping layer deposition should be less than one day (24 hours) in order to reduce CuO formation.

The process of the present invention reduces copper hillock formation by reducing the sensitivity of the copper surface to the deposition environment and by reducing the CuO presence. This is achieved by: 1) pre-coating an oxide layer on the deposition chamber walls, 2) using NH_3 plasma rather than NH_3 gas in the deposition chamber, and 3)

keeping the time between copper CMP and capping layer deposition to less than one day (24 hours).

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is: